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SUPPORT FOR VERTICALLY-ORIENTED CAPACITORS DURING THE FORMATION OF A SEMICONDUCTOR DEVICE

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SUPPORT FOR VERTICALLY-ORIENTED CAPACITORS DURING THE FORMATION OF A SEMICONDUCTOR DEVICE

Field of the Inventi n

[0001] This invention relates to the field of semiconductor manufacture and, more particularly, to a method for forming a double-sided capacitor having lateral support for its capacitor bottom plate.

Background of the Invention

[0002] During the manufacture of semiconductor devices which comprise memory elements, such as dynamic random access memories (DRAMs), static random access memories (SRAMs), and some microprocessors, capacitors such as container capacitors and pedestal capacitors are commonly formed. Container and pedestal capacitors are well known to allow an increased stored charge over planar capacitors by increasing the surface area on which the charge may be stored.

[0003] FIGS. 1-7 depict a conventional method for forming a plurality of container capacitors from polysilicon. Formation of a pedestal capacitor is similar, but the bottom plate is a solid plug and the cell dielectric and top plate are conformal with the exterior of the bottom plate to form a single-sided vertically-oriented capacitor. FIG. 1 depicts a semiconductor wafer substrate assembly 10 comprising a semiconductor wafer 12 having a plurality of doped source/drain regions 14 within the wafer 12. FIG. 1 further depicts transistors 16 comprising gate oxide 18, a doped polysilicon control gate 20, silicide 22 such as tungsten silicide which increases conductivity of the control gate 20, and a capping layer 24 often manufactured from silicon nitride. Silicon nitride spacers 26 are formed to insulate the control gate 20 and silicide 22 from polysilicon pads 28 to which the container capacitors will be electrically coupled. Shallow trench isolation (STI, field oxide) 30 reduces unwanted electrical interaction between adjacent control gates. An etch stop

layer 31 is formed, then a thick layer of deposited oxide 32 such as borophosphosilicate glass (BPSG) formed to provide a base dielectric layer for capacitor features which are formed later. A patterned photoresist layer 34 defines the location of the container capacitors to be formed. The FIG. 1 structure may further include one or more bit (digit) lines under the BPSG layer or various other structural elements or differences which, for simplicity of explanation, have not been depicted.

[0004] The FIG. 1 structure is subjected to an anisotropic etch which removes the exposed portions of the BPSG layer to expose the etch stop layer 31 and to form a patterned BPSG layer which provides a base dielectric having recesses for the capacitors. The exposed portion of the etch stop is the removed. Subsequent to the etch of etch stop 31 the polysilicon pads 28 and possibly a portion of capping layer 24 are exposed to result in a structure similar to FIG. 2. The remaining photoresist layer 34 is stripped and any polymer (not depicted) which forms during the etch is removed according to means known in the art to provide the FIG. 3 structure.

[0005] As depicted in FIG. 4, a blanket conductive layer 40 such as polysilicon or another material is formed conformal with the deposited oxide layer, and will provide a capacitor storage node for the completed capacitor. A thick blanket filler material 42, such as photoresist, is formed to fill the containers provided by polysilicon 40. The FIG. 4 structure is then subjected to a planarizing process, such as a chemical planarization, a mechanical planarization, or a chemical mechanical planarization (CMP) step. This process removes portions of the photoresist 42, the polysilicon 40, and usually a portion of the BPSG 32 to result in the FIG. 5 structure.

[0006] Next, the BPSG 32 is partially etched with an etch selective to polysilicon (i.e. an etch which minimally etches or, preferably, doesn't etch polysilicon) to result in the structure of FIG. 6. At this point in the process the polysilicon storage nodes (capacitor bottom plates) 40 are only minimally

supported. The bottom plates 40 in the FIG. 6 structure each comprise a first region 60 which defines a recess, and a second region 62 which defines an opening to the recess, with the first and second regions being continuous, each with the other. In other words, the bottom plate 40 of FIG. 6 defines a receptacle having a rim 62 which defines an opening to the interior of the receptacle. The regions 60, 62 form vertically-oriented sides of the bottom plate, and the sides are electrically-coupled by a horizontally-oriented bottom 64.

[0007] Next, a cell dielectric layer 70, for example a layer of high-quality cell nitride, a polysilicon container capacitor top plate 72, and a planar oxide layer such as BPSG 74 are formed according to means known in the art to result in the FIG. 7 structure. This forms a "double-sided" capacitor, as both the capacitor cell dielectric 70 and capacitor top plate 72 follow the contours of the majority of both the inside and outside of each container capacitor bottom plate 40. After forming the structure of FIG. 7, wafer processing continues according to means known in the art.

[0008] It can be seen at the FIG. 6 structure that conventional processes remove the oxide 32 which supports the capacitor bottom plate 40. This oxide removal is performed to allow formation of the cell dielectric and capacitor top plate on both sides of the bottom plate to form a double-sided capacitor. The structure of FIG. 6 is easily damaged and susceptible to defects such as leaning (caused, for example, during the etch of BPSG 32 of FIG. 5 to result in FIG. 6), toppling, or lifting of the bottom plate. However, it is desirable to form a double-sided capacitor to increase the cell capacitance which allows the cell height to be decreased over a single sided capacitor. Limiting this vertical dimension of the cell capacitor is desirable because it sets the depth of the contact level to follow. For example, current etch tool technology can etch contacts to a depth of about 3.0 micrometers (μm) to about 3.5 μm. If the capacitor height causes the contact depth to go beyond the 3.0 μm to 3.5 μm limit, then additional masking layers will be needed.

One way to do this is to form a portion of the contact to diffusion areas in the wafer before forming the capacitor, then forming the remaining portion after forming the capacitor. Such a process is complex and adds significantly to device cost.

[0009] Another problem which can occur during conventional processing results indirectly from the etch of BPSG layer 32 of FIG. 5 to result in the FIG. 6 structure. During this etch, BPSG over the device periphery (not depicted) is also etched, which forms a step in the oxide between the periphery, where there are no cell capacitors, and the array, where the tops of the cell capacitors are at the original level of the top of BPSG 32. After forming the cell dielectric and top plate, the periphery region must be backfilled with oxide, which is then planarized. The requirement to backfill and planarize results in additional processing steps, which contributes to a further increase in costs.

[0010] A method used to form a double-sided capacitor such as a container capacitor or a pedestal capacitor which reduces or eliminates one or more the problems described above, and a structure resulting therefrom, would be desirable.

Summary of the Invention

[0011] An embodiment of the present invention provides a new method which, among other advantages, reduces problems associated with the manufacture of semiconductor devices, particularly problems resulting from instability of unsupported capacitor bottom plates prior to formation of a supporting layer.

[0012] Various embodiments of the present invention provide lateral support for a vertically-oriented structure, for example a storage capacitor such as a container capacitor or a pedestal capacitor.

[0013] Additional advantages will become apparent to those skilled in the art from the following detailed description read in conjunction with the appended claims and the drawings attached hereto.

Brief Description of the Drawings

[0014] FIGS. 1-7 are cross sections depicting a conventional method for forming a double-sided container capacitor structure;

[0015] FIGS. 8-16 and 18-20 are cross sections, and FIG. 17 is a plan view, depicting embodiments of the inventive method for forming a double-sided container capacitor structure;

[0016] FIGS. 21 and 22 are cross sections depicting an embodiment of the invention to form a pedestal capacitor;

[0017] FIG. 23 is a block diagram of an exemplary use of the invention as a memory array in a dynamic random access memory; and

[0018] FIG. 24 is an isometric depiction of a use of the invention in an electronic device.

[0019] It should be emphasized that the drawings herein may not be to exact scale and are schematic representations. The drawings are not intended to portray the specific parameters, materials, particular uses, or the structural details of the invention, which can be determined by one of skill in the art by examination of the information herein.

Detailed Description of the Preferred Emb diment

[0020] The term "wafer" is to be understood as a semiconductor-based material including silicon, silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. Furthermore, when reference is made to a "wafer" in the following description, previous process steps may have been utilized to form regions or junctions in or over the base semiconductor structure or foundation. Additionally, when reference is made to a "substrate assembly" in the following description, the substrate assembly may include a wafer with layers including dielectrics and conductors, and features such as transistors, formed thereover, depending on the particular stage of processing. In addition, the semiconductor need not be silicon-based, but could be based on silicon-germanium, silicon-on-insulator, silicon-on-sapphire, germanium, or gallium arsenide, among others. Further, in the discussion and claims herein, the term "on" used with respect to two layers, one "on" the other, means at least some contact between the layers, while "over" means the layers are in close proximity, but possibly with one or more additional intervening layers such that contact is possible but not required. Neither "on" nor "over" implies any directionality as used herein.

[0021] A first embodiment of an inventive method used during the formation of a semiconductor device, and various inventive in-process structures, are depicted in FIGS. 8-20. FIG. 8 depicts a structure comprising a semiconductor wafer substrate assembly 10 comprising a semiconductor wafer 12, conductively-doped regions 14 within the wafer, transistors comprising gate oxide 18, a word line 20, silicide 22 which enhances conductivity of the word line, a dielectric transistor capping layer 24, dielectric spacers 26, and conductive contact pads 28. The contact pads 28 reduce the amount of dielectric which must be removed during an etch of an overlying dielectric layer.

[0022] After forming the features of the wafer substrate assembly 10, a blanket etch stop layer 31 is formed. The etch stop layer 31 may comprise a layer of silicon nitride, silicon carbon (Si•C), aluminum oxide (Al_2O_3), or another material between about 50 angstroms (Å) and about 1,000 Å thick. Next, a base dielectric layer 84, for example borophosphosilicate glass (BPSG), phosphosilicate glass (PSG), spun-on dielectric (SOD), or undoped silicate glass (USG), is formed over etch stop layer 31. A blanket support layer 86 and a blanket sacrificial layer 88 are formed over the base dielectric layer 84. Properties of support layer 86 and sacrificial layer 88 include etchability of layers 88 and 84 selective to layer 86 (i.e. layers 88 and 84 can be etched while removing none or very little of layer 86). Layer 86 may comprise a second silicon nitride layer between about 200 Å and about 1,200 Å thick, and layer 88 can comprise a silicon dioxide layer, for example using a BPSG or tetraethyl orthosilicate (TEOS) process, between about 300 Å and about 600 Å thick, preferably about 400 Å. Next, a patterned etch mask 90 is formed having openings therein which allow an etch to expose contact pads 28.

[0023] After forming mask layer 90, the structure of FIG. 8 is etched to remove the exposed portions of sacrificial layer 88, support layer 86, base dielectric layer 84, and etch stop layer 31, and to expose contact pads 28 and possibly a portion of capping layer 24 to result in a structure similar to FIG. 9. A single etch can initially be used to remove exposed portions of sacrificial silicon dioxide layer 88, silicon nitride support layer 86, and timed to stop within base dielectric layer 84 prior to exposing etch stop 31. The chemistry can then be changed so that any remaining base dielectric layer 84 is removed while stopping on etch stop 31. Then, optionally, the etch can be changed and performed for a time to sufficiently remove exposed portions of etch stop 31 which exposes contact pad 28, while not excessively etching capping layer 24 or spacers 26. The etch stop layer 31 may also be left in place.

[0024] After forming the FIG. 9 structure, photoresist layer 90 is removed, along with any polymer (not depicted) or other contaminants which form during the etch, to result in the structure of FIG. 10.

[0025] Next, a blanket conformal capacitor bottom plate layer 110 such as titanium nitride is formed as depicted in FIG. 11. A protective layer 112 such as photoresist, is formed within the container to prevent contaminants from being deposited into the interior of the container formed by the bottom plate during subsequent processing. After forming bottom plate layer 110 and protective layer 112, the structure is planarized, for example using chemical mechanical planarization (CMP) to result in the FIG. 12 structure.

[0026] After forming the structure of FIG. 12, sacrificial layer 88 is selectively etched to expose the underlying support layer 86, then protective layer 112 is removed. For example, a sacrificial layer 88 of silicon dioxide can be etched selective to a silicon nitride support layer 86 and a titanium nitride bottom plate layer 110 using a wet etch comprising hydrofluoric acid (HF). Likewise, a protective layer 112 of photoresist can be removed by ashing the material at a temperature of between about 150°C and about 300°C, and then subjecting the ash to a wet etch, for example using hydrofluoric acid (HF) to remove the photoresist ash. The etch of the sacrificial layer 88 can be performed either before or after removal of protective layer 112, if the etch is selective to the material of bottom plate 110. If the etch of layer 88 is performed after removal of layer 112, the etchant may traverse any pinholes or other voids within bottom plate layer 110 and begin to etch oxide layer 84. This is not detrimental, however, as layer 84 will be removed during subsequent processing and provides no further critical function. The removal of protective layer 112 and sacrificial layer 88 results in the FIG. 13 structure.

[0027] Next, a masking spacer layer 140 is formed over the surface of the FIG. 13 structure to result in the structure of FIG. 14. The material selected for this layer must be able to withstand an etch of support layer 86, and must also be etchable selective to the material of support layer 86 and bottom plates 110. With a nitride support layer and titanium nitride bottom plates, polysilicon would function sufficiently. The masking spacer layer is formed to a thickness sufficient to fill in and impinge on itself in narrow regions 142, and form conformally in the wider regions 144. With current technology, the narrow regions 142 may have a width of between about 200 Å and about 600 Å, the wider regions 144 may have a width of between about 600 Å and about 1,200 Å. The height of the exposed portions 146 of capacitor bottom plates 110, which is determined by the thickness of sacrificial layer 88, is between about 300 Å and about 600 Å. To result in the structure of FIG. 14, a conformal polysilicon layer 140 is formed to have a target thickness of between about 200 Å and about 500 Å when measured over wide, flat surfaces. FIG. 14 depicts layer 140 completely filling the recess in the bottom plates, but this may not occur, depending on the size of the opening within the bottom plate. However, enough material will likely form to prevent any damage to the bottom of plates 110 during a subsequent spacer etch of layer 140 described below.

[0028] Next, an anisotropic spacer etch is performed on the masking spacer layer 140 to result in the FIG. 15 structure. This etch removes the material of the masking spacer layer 140 selective to the material of support layer 86 and bottom plates 110. After etching layer 140, spacers 150 remain in the wider regions 144, while layer 152 remains to bridge the narrow regions 142 formed by adjacent bottom plates 110.

[0029] After forming spacers 150, the support layer 86 is etched using the spacers 150 and the other remaining portions 152 of layer 140 as a mask to result in the FIG. 16 structure. FIG. 16 is depicted in plan view along 1-1 of FIG. 17, which depicts part of an array of container capacitor bottom plates

110 and the remaining portions 150, 152 of the masking spacer layer 140. Various capacitor layouts other than the one depicted in FIG. 17 can be used with the present invention. As this pattern of the masking layer defines the support layer 86, the configuration of the support layer 86 is analogous to that of the masking spacer layer of FIG. 17. The etch of the support layer 86 with this mask removes the material of support layer 86 selective to the material of bottom plates 110. The spacers 150 and support layer 86 can also be etched during the same operation, but it is more likely that the spacers 150 will be etched during one process and the support layer 86 will be etched during another separate etch. During the etch of support layer 86 a portion of polysilicon layer 140 and spacers 150 may also be removed, as long as enough of these two features remain to allow exposure of BPSG 84 in the wide regions 144 and protection of support layer 86 in the narrow regions 142.

[0030] The remaining portions 140, 150, and 152 of the masking spacer layer can be removed at this point to result in the structure of FIG. 18, or they may remain in place. If polysilicon spacers are removed, they can be etched selective to silicon nitride support layer 86 and titanium nitride bottom plates 110 using a wet etch comprising tetramethyl ammonium hydroxide (TMAH).

[0031] FIG. 19 depicts the structure resulting from the removal of polysilicon features 140, 150, and 152, and after etching of base dielectric layer 84. The base dielectric layer is removed selective to support layer 86, bottom plates 110, and etch stop 31. An etch which removes silicon dioxide selective to silicon nitride and titanium nitride includes a wet etch of hydrofluoric acid (HF) to result in the structure of FIG. 19. The etchant completely removes the exposed base dielectric layer 84 depicted in FIG. 17, and removes all of dielectric 84 around each capacitor bottom plate 110.

[0032] As depicted in the FIG. 19 structure, support structures 86 support the capacitors after removal of the base dielectric layer 84. Removal of the base dielectric layer is necessary to allow the formation of a double-sided capacitor. These support structures provide a dielectric collar for each bottom plate, with each collar being continuous with adjacent collars such that the support layer forms a matrix which braces all capacitor bottom plates. The arrangement of the support layer can be determined from FIG. 17, which depicts the pattern of masking spacer layer 150, 152, and also of the etched support layer 86. As depicted in FIG. 19, the top and bottom surfaces of support layer 86 are free from contact with any other layer. However, some of dielectric 84 may remain, especially at the point of contact between the support layer 86 and the bottom plate 110, which may be more difficult to clear completely. In any case, even if some of this dielectric 84 remains to contact the bottom side of layer 86, the top and bottom surface of support layer 86 will remain generally free from contact with any other layer. It is conceivable that for some capacitor arrangements and processes the collar may not surround the capacitor bottom plate through 360° as depicted in FIG. 17. Further, the bottom plates or other feature being supported by the collar may not be circular as depicted in FIG. 17, but may be oval, ovoid, square, rectangular, etc. in shape.

[0033] If the remaining portions 150, 152 of spacer layer 140 have not yet been removed, they must be removed at this point to prevent shorting between capacitor bottom plates.

[0034] Finally, a capacitor cell dielectric 200, a capacitor top plate 202, and a dielectric layer 204 are formed according to means known in the art to form the structure of FIG. 20. Wafer processing continues according to means known in the art.

[0035] The completed structure may have improved capacitance over conventional structures, because all of the base dielectric layer can be removed which allows the top plate to be formed along more of the bottom plate than conventional structures. Referring to FIG. 6, for example, a portion of base dielectric layer 32 must remain in place to support the capacitors during formation of the cell dielectric and top plate. With an embodiment of the present invention, however, all of the base dielectric layer can be removed as depicted in FIG. 19, because support layer 86 remains to brace the bottom plates.

[0036] To prevent etching of the periphery, a mask layer may be formed prior to the etch of the sacrificial dielectric layer, prior to the etch of the masking spacer layer, or prior to the etch of the support layer. This will prevent etching of BPSG over the device periphery, which would form a step in the oxide between the periphery, where there are no storage cell capacitors, and the array, where the tops of the storage cell capacitors are at the original level of the top of layer 88. If the periphery is not protected, the periphery must be backfilled with oxide which is then planarized, after forming the cell dielectric 200 and top plate 202.

[0037] A selective etch may be performed on support layer 86 after forming spacers 152 of FIG. 16 to increase the width of the opening at 144. This larger opening may allow the base dielectric layer to be more easily removed, and may provide improved conditions for forming the cell dielectric layer 200 and capacitor top plate 202.

[0038] A pedestal capacitor can be formed in a manner similar to the container capacitor as depicted by FIGS. 21 and 22. As depicted in FIG. 21, the bottom plate layer 110 is formed to completely fill the recessed defined by the sacrificial layer 88, the support layer 86, and the base dielectric layer 84. Thus the bottom plate layer 110 will be much thicker than that depicted in the FIG. 11 structure. In this pedestal capacitor embodiment, protective layer 112 is not necessary, as bottom plate layer 110 completely fills the

recess. After forming the FIG. 21 structure, the bottom plate layer 110 and possibly a portion of the sacrificial layer 88 is planarized to remove layer 110 from the horizontal surface of sacrificial layer 88 to leave the pedestal capacitor bottom plate 110 as depicted in FIG. 22.

[0039] In another embodiment, a single layer of material may be formed instead of forming both the sacrificial layer 88 and the support layer 86 of FIG. 12. This single layer would be a thicker layer of the material of the support layer, such as silicon nitride, and would be as thick as layers 86 and 88 combined. A timed etch would be performed on this layer to result in the structure of FIG. 13. This process is not as controllable as using two separate layers and is therefore not as preferable for most process flows, but may have advantages for some processes. Processing then continues according to the other embodiments, for example to form the masking spacer layer 140 and other subsequent steps.

[0040] With the above embodiments of the invention it may be necessary to protect the peripheral area of the die during processing of the array of capacitors, especially during the etch of the base dielectric of the FIG. 18 structure to form the FIG. 19 structure. FIG. 23 is a plan view depicting four arrays 230 and a periphery 232 of a semiconductor die 234 prior to forming the patterned resist layer 90 of FIG. 8. A typical memory die will likely comprise a larger number of arrays.

[0041] FIG. 24 depicts the FIG. 23 structure after forming patterned photoresist layer 90. Resist layer 90 has openings therein 240 which will allow the etch of the sacrificial layer 88, the support layer 86, and the base dielectric layer 84 of the FIG. 8 structure to form the FIG. 9 structure. FIG. 24 is not to scale, and many more openings 240 for capacitors will be formed than are depicted. Resist layer 90 also has openings therein 242 which form a "moat" around the array which will protect the periphery 232 during the removal of base dielectric layer 84 to form the FIG. 19 structure. This moat will be filled with material during the formation of the capacitor

bottom plate 110, and thus no additional processing is required to form and fill the moat. For current processing, the moat may be between about 200 Å and about 600 Å wide. During the etch of the base dielectric through the collar, a photoresist layer would be formed to cover and protect the periphery but to expose the array. The photoresist layer and the layer within the moat thereby protects the dielectric layer such as BPSG in the periphery from being etched during the removal of the base dielectric layer which exposes the sidewalls of the capacitor bottom plates.

[0042] As depicted in FIG. 25, a semiconductor device 250 formed in accordance with the invention may be attached along with other devices such as a microprocessor 252 to a printed circuit board 254, for example to a computer motherboard or as a part of a memory module used in a personal computer, a minicomputer, or a mainframe 256. FIG. 25 may also represent use of device 250 in other electronic devices comprising a housing 236, for example devices comprising a microprocessor 252, related to telecommunications, the automobile industry, semiconductor test and manufacturing equipment, consumer electronics, or virtually any piece of consumer or industrial electronic equipment.

[0043] The process and structure described herein can be used to manufacture a number of different structures which comprise a capacitor such as a container capacitor or a pedestal capacitor. FIG. 26, for example, is a simplified block diagram of a memory device such as a dynamic random access memory having a memory array with container capacitors which may be formed using an embodiment of the present invention. The general operation of such a device is known to one skilled in the art. FIG. 26 depicts a processor 260 coupled to a memory device 262, and further depicts the following basic sections of a memory integrated circuit: control circuitry 264; row 266 and column 268 address buffers; row 270 and column 272 decoders; sense amplifiers 274; memory array 276; and data input/output 278.

[0044] While this invention has been described with reference to illustrative embodiments, this description is not meant to be construed in a limiting sense. Various modifications of the illustrative embodiments, as well as additional embodiments of the invention, will be apparent to persons skilled in the art upon reference to this description. It is therefore contemplated that the appended claims will cover any such modifications or embodiments as fall within the true scope of the invention.